HIGH PERFORMANCE COMPUTING MODERNIZATION PROGRAM

RESEARCH PROJECT #: HPCMP-HIP-24-028

Physics of Electron Emission from Semiconductor Surfaces

About AFRL:

Air Force Research Laboratory (AFRL) is a scientific research organization operated by the United States Air Force Materiel Command. AFRL is dedicated to leading the discovery, development, and integration of aerospace warfighting technologies, planning, and executing the Air Force science and technology program, and providing warfighting capabilities to United States air, space, and cyberspace forces.

The electronic materials research team at the Materials and Manufacturing Directorate is focused on the development of next generation electronic materials for use in a wide variety of Air Force systems and applications such as RF amplification, high power electronics, and quantum computing.

RESEARCH LOCATION: Wright-Patterson AFB, OH

PROJECT DESCRIPTION:

Research will involve the physics of electron emission processes from semiconducting surfaces. Ab-initio calculations will be used to determine fundamental electronic properties of semiconducting surfaces. These results will be used with recently developed computational methods for determining emission currents, where both thermal and field emission are considered. This research will enable the development of vacuum field effect transistors (vacFET). VacFET devices have the potential to operate at higher cut off frequencies, are potentially radiation hardened, and can also operate at atmospheric pressure. These properties make vacFET devices ideal for use in extreme environments such as those present in a space environment.

This research will consist of essentially two stages. The first will involve initial DFT calculations performed on ideal single crystal surfaces. Gallium Nitride (GaN) and Silicon Carbide (SiC) single crystal surfaces will be of interest. Having atomically smooth surface is critical for the electron emission process. Part of the fabrication of these devices will involve selective etching for certain crystal faces with the intent of optimizing electron emission. DFT will allow us to accurately calculate fundamental properties such as work function and density of states as well as potential barriers of the etched surfaces. The second stage will involve combining DFT results with existing computational methods developed by the team. Results will give us significant insight on how well this process is working and what to expect in term of current density. Modeling and simulation will exist in a feedback loop with device fabrication which in turn is expected to accelerate results. These results will play an important role in evaluating device performance.

The interns will be expected to research within an existing team on the development vacuum channel transistors. This team consists of multiple researchers in both the Materials and Manufacturing and Sensors directorates. Research will consist of initial DFT calculations on model systems. Once completed, these results will be integrated into existing computational code developed by the research team. Additionally, developments made with modeling and simulation will be used to evaluate/compare both two and three terminal devices being fabricated by the research team. Research will be presented to the research team on a bi-weekly basis at group meetings.

ANTICIPATED START DATE:

May 2024 – Exact start dates will be determined at the time of selection and in coordination with the selected candidate.

QUALIFICATIONS:

The ideal candidate will have a strong background in solid state physics and should also have knowledge of computational methods for determining the electronic structure of semiconductor materials. Previous experience with DFT calculations on VASP and/or Quantum Espresso is highly desired.

ACADEMIC LEVEL:

Degree received within the last 60 months or currently pursuing:

- Master's
- Doctoral

DISCIPLINE NEEDED:

- Computer, Information, and Data Sciences
- Engineering
- Physics
- Science & Engineering-related